

Application No.:10/084,810
Docket No.:JCLA4426-D

In the Specification

Please amend the paragraph on page 11, line 9 as follow :

As shown in Fig. 2H, using the electroplate layers 208b and the circuit line mask 226 as an etching mask, the exposed surface 202b of the metal substrate 200 is etched. During the etching operation, a portion of the metal substrate 200 is removed exposing a portion of the insulating material 224 to form external metal pegs 230 and printed circuit lines 228. Hence, a package having an array of metal pegs connected by printed circuit lines is formed. After the etching operation, the die pad 212 has a profile with its lower surface 216b at the same level as the underside of the package. The metal external metal pegs 230 are electrically connected to the internal metal pegs 214 via the printed circuit lines 228 (not shown in Figure 2H). Alternatively, the external metal pegs 224230 and the internal metal pegs 214 can be electrically connected directly without the need of a circuit line.

Please amend the paragraph on page 11, line 20 as follow:

As shown in Fig. 2H, the package structure of this invention includes at least a die pad 212 with a silicon die 220 on its upper surface 216a. The lower surface 216b of the die pad 212 is exposed. The external pegs 230 are positioned around the die pad 212 area forming an area array layout. One end of each internal metal peg 214 is buried inside the insulating material 224 of the package and is electrically connected to a bonding pad on the die 220. The other end of the metal peg 214 is connected to a printed circuit line 228 (not shown in Figure 2H) so that the internal metal peg 214 is electrically connected to an external metal peg 224230 via the circuit

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line 228 (not shown in Figure 2H). However, an internal metal peg and an external metal peg 228230 can also be electrically connected directly. In addition, the end face of each internal metal peg 214 has an electroplate layer 208a. Similarly, the end face of each external metal peg 224230 also has an electroplate layer 208b. These electroplate layers 208a and 208b are convenient locations for carrying out electrical connection, molding and subsequent soldering process.